18. (New) A semiconductor device according to claim 16 wherein said second well is formed on only one side of said second region with reference to [a] said predetermined boundary.

19. (New) A semiconductor device according to claim 18 wherein said second well is formed in a memory cell part in said second region.

20. (New) A semiconductor device according to claim 1, wherein each of the first wells has a single element formed therein.

21. (New) A semiconductor device according to claim 13, wherein each of the first wells has a single element formed therein.

22. (New) A semiconductor device according to claim 15, wherein each of the first wells has a single element formed therein.

23. (New) A semiconductor device according to claim 16, wherein each of the first wells has a single element formed therein.

IN THE ABSTRACT OF THE DISCLOSURE

The following is a clean copy of the abstract at page 29, lines 1-10, with a marked-up copy attached.

A semiconductor device including a well divided into a plurality of parts by a trench, to effect a reduction in layout area, and a manufacturing method thereof. In the semiconductor device, an element isolation film is formed such as to have to a depth from the main surface of a semiconductor substrate, and the area from the main surface of the substrate to the depth is divided into a plurality of first regions. A first well is formed in each of the first regions. A second well is formed in a second region deeper than the first well in the substrate, and the second well is in contact with some of the first wells.